
TC-432/582 SMARTOPS
DESCRIPTION AND OPERATIONS GUIDE
Version 1.1 02/20/97

TABLE OF CONTENTS

- 1.0 SmartOps Functional Description
- 2.0 Connectors
- 3.0 Memory Map
- 4.0 Trigger Messages to TC-432/582
 - 4.1 Lines
- 5.0 Trigger Messages from TC-432/582
- 6.0 Pin and Port Assignments
- 7.0 Configuration Jumpers

This document is intended for the installation and support of Show Control Systems supplied by Triad Productions, Inc. and contains trade secret information regarding proprietary inventions and processes. This information may not be duplicated or revealed in any form without express permission of Triad Productions, Inc.

© 1989-1999 William J. Synhorst/Triad Productions, Inc. All rights reserved.

We believe this information to be correct and accurate at the time of printing. All specifications are subject to change. Triad will not be responsible for any damage related to any use of this equipment or documentation. Please report errors or omissions to Triad Productions, Inc.

SECTION 1.0 FUNCTIONAL DESCRIPTION

The TC-432/582 SmartOps board set is designed to integrate a number of common I/O functions into a local processor to solve many typical control I/O applications (especially Operator Panels). It requires only a single serial connection to a Show Control Unit and 24VDC for power thus freeing up digital I/O points and reducing wiring cost and labor.

The board provides for serial communications to a BART, LDC, PC running Synthesis, or any other RS-232 serial device. It also provides feedback/messaging via an optional two line by 16 character, back-lit LCD display. The board also provides 32 digital switch closure inputs and 32 digital outputs rated at 100 ma maximum which is sufficient for indicator lamps or relays.

Inputs and outputs can be used to control the selection of "real world" aspects from external inputs, which makes the SmartOps ideal for intelligent operator controls or interactive displays. The two line LCD display adds a way to give meaningful feedback to operators in ways that would be impossible with standard digital I/O.

The SmartOps board set is designed primarily for remote operator panel interface but may also be used as a generic remote input/output device.

SECTION 2.0 CONNECTORS

Connections to the outside world are all made on the TC-432 I/O board.

Power A screw type terminal (JP6) for easy field termination.

Serial A screw type terminal (JP6) for easy field termination.

Digital Input Split across two 40 pin connectors (JP12 and JP13).

Digital Output Split across two 40 pin connectors (JP1 and JP2).

See Section 6.0 (Pin and Port Assignments) for details.

SECTION 3.0 MEMORY MAP

The 68HC11F processor has a very flexible I/O mapping capability and we have attempted to map all I/O, RAM, ROM, and EE ROM to provide optimal use of each.

In order to make use of the "page 0" instructions and utilize all of the available 1k of internal RAM, we are mapping it in the range of \$0000 to \$03FF.

The internal registers (64) are mapped starting at \$1000 to allow full use of the RAM, albeit giving up page 0 addressing to them. External I/O is decoded from \$1060 to \$17FF.

The internal EE ROM is mapped in two pages, from \$7E00 to \$7FFF, again so that all 512 bytes are available for user applications, including parameters, configuration, or other semi-permanent/field changeable data.

The entire space of \$8000 to \$FFFF (32k) is available for an external EPROM, Flash ROM, or other device, and is intended to be the primary program storage area. Although a 256k device would be fully available, larger devices may be configured through a bank-switching mechanism, allowing multiple applications to be available without having to exchange EPROMs in the field. All of the vectors (reset, IRQs, etc.) must always reside at the very top of this area.

FFFE/FFFF	RESET
FFFC/FFFD	
FFFA/FFFB	
FFF8/FFF9	ILL OPCODE
FFF6/FFF7	SWI
FFF4/FFF5	XIRQ
FFF2/FFF3	IRQ
FFF0/FFF1	RTI (real time int)
FFEE/FFEF	
FFEC/FFED	
FFEA/FFEB	
FFE8/FFE9	
FFE6/FFE7	
FFE4/FFE5	
FFE2/FFE3	
FFE0/FFE1	

7E00-7EFF	EE PROM
------------------	---------

1000-103F	Internal registers
0100-03FF	Internal RAM
0000-00FF	Internal RAM with page 0 addressing

For the TC-432(A) I/O card, the following external addresses are decoded:

	WRITE		READ
1400	Outputs 1-8		1-4+
1420	Outputs 9-16		5-8+
1440	Outputs 17-24		
1460	Outputs 25-32		
1480	Outputs 33-40	TTL/LCD	
14E0	Data Latch	LCD	

BIT	7	6	5	4	3	2	1	0
FUNC	SonAlrt	Backlit	Usr	Usr	Usr	LCD RS	LCD RW	LCD EN

SCI BAUD RATES

250k	TRX Remote I/O
38.4	?? May not be available
31.25	MIDI
19.2	Network RS-485 Bi-Directional
9600	Dedicated RS-232 serial/local
2400	Long Distance RS-232

SECTION 4.0 TRIGGER MESSAGES TO TC-432/582

All serial communication is performed at 8 data bits, no parity, 1 stop bit at one of the above defined baud rates, depending on the hardware and installation specific configuration required. Trigger messages follow the basic protocol of Synthesis, using lead-in characters that will not interfere with "TriCode" time code data.

LEAD-IN DEC	HEX	TRIGGER USE	DESCRIPTION
240	\$F0	Macro #	<Message in ASCII> 255
* 241	\$F1	Port (1)	<Message in ASCII> 255 - redirect message SWUART
* 242	\$F2	Macro #	; recall message number in LINE* to line
* 243	\$F3	Port (1)	MSG# ;recall stored message to UART
* 248	\$F8	N/A	ACK - Reserved for handshake
* 249	\$F9	N/A	NAK - Reserved for handshake
* 251	\$FB	*	Value, X Var
* 252	\$FC	N/A	Enter Terminal Mode
253	\$FD	N/A	Reset System
254	\$FE	1-40	Output 1-40 on (latched)
		65-104	Output 1-40 off (latched)
		41	Flash = Pulse (1 Shot), Fast
		42	Flash = Pulse (1 Shot), .5 Second
		43	Flash = Pulse (1 Shot), 1 Second
		44	Flash = Pulse, User Defined
		45	Flash = 50% Duty Cycle, Fast
		46	Flash = 50% Duty Cycle, Medium
		47	Flash = 50% Duty Cycle, Slow
		...	other duty cycles, rates
		129-168	Flash Output at last selected rate
* 255	\$FF	TBD	Start/Clear counter timers
		N/A	Closes any open communication (terminal/string)

SECTION 4.1 LINES

***** NOTE - LINE MEMORIES NOT CURRENTLY SUPPORTED *****

Up to sixteen (16) lines of 32 characters may be defined for local, RAM storage of ASCII macro text. For a two line display, odd lines (1,3, etc.) are displayed on the top line, while even lines are displayed on the bottom line. Normally, any messages would be sent to line 1 or 2, and be immediately displayed and stored in line memories 1 and 2 respectively. Any other line number is available for up to 16 local RAM memories that can be recalled with a shorter message (type 242, LINE).

MEMORY LINE	DISPLAY 2 LINE	DISPLAY 4 LINE
1	1	1
2	2	2
3	1	3
4	2	4
5	1	1
6	2	2
7	1	3
8	2	4
9	1	1
10	2	2
11	1	3
12	2	4
13	1	1
14	2	2
15	1	3
16	2	4

An alternative is to have 16 line memories with a display line attribute for each, so that any message can go to any line.

Messages may also be stored in FLASH ROM (up to 16, 32 characters, max.) or in the primary program memory (ROM/Flash).

SECTION 5.0 TRIGGER MESSAGES FROM TC-432/582

For FULL DUPLEX applications, the following is planned for messages from the remote I/O back to the host.

Note: The format is nearly identical to the incoming messages, so that by connecting a loop-back connector, the system can be easily tested.

LEAD-IN	HEX	TRIGGER	DESCRIPTION	
		USE		
*	240	\$F0	Macro #	<Message in ASCII> 255 (from remote keyboard)
*	241	\$F1	Port (1)	<Message in ASCII> 255 - redirect message SWUART
*	248	\$F8	N/A	ACK - Reserved for handshake
*	249	\$F9	N/A	NAK - Reserved for handshake
*	251	\$FB	*	Value, X Var
*	253	\$FD	N/A	Reset System
	254	\$FE	1-40	Input 1-40 on
			65-104	Input 1-40 off (latched)
			TBD	Counter / timers
*	255	\$FF	N/A	Closes any open communication (terminal / string)

For Half-Duplex/network applications, suitable changes will need to be implemented to prevent return traffic from being mis-interpreted.

X-VARIABLES

32 (64?) "X" variables are defined that can be used for mode and status flags, message values, variable strings, and counters or timers. (NOT IMPLEMENTED YET!)

MACRO STRINGS REVEALED

The following "features" apply to macro strings, in the format that is very similar to a subset of other Triad Synthesis SCU/LDC formats:

/nnn - use as ASCII character to display or send (allows 000-255)

/nnx - use x(nn) as ASCII representation of number. (if x(1) = 5 then /01x would "parse" to "05")

/nnX - use x(nn) as ASCII character. (if x(1) = 65 then /01X would "parse" to "A")

\comment - terminates line

SECTION 6.0 PIN AND PORT ASSIGNMENTS**JP1**

**40 Pin Dual Row Header
Digital Output - Bank 1 (1-16)
Pins 1-16 24VDC Buss**

1	Output 1	21
2	Output 2	22
3	Output 3	23
4	Output 4	24
5	Output 5	25
6	Output 6	26
7	Output 7	27
8	Output 8	28
9	Output 9	29
10	Output 10	30
11	Output 11	31
12	Output 12	32
13	Output 13	33
14	Output 14	34
15	Output 15	35
16	Output 16	36
17	Unused	37
18	Unused	38
19	Unused	39
20	Unused	40

JP2

**40 Pin Dual Row Header
Digital Output - Bank 2 (17-32)
Pins 1-16 24VDC Buss**

1	Output 17	21
2	Output 18	22
3	Output 19	23
4	Output 20	24
5	Output 21	25
6	Output 22	26
7	Output 23	27
8	Output 24	28
9	Output 25	29
10	Output 26	30
11	Output 27	31
12	Output 28	32
13	Output 29	33
14	Output 30	34
15	Output 31	35
16	Output 32	36
17	Unused	37
18	Unused	38
19	Unused	39
20	Unused	40

JP12
40 Pin Dual Row Header
Digital Input - Bank 1 (1-16)
Pins 21-36 Common Buss

1	Input 1	21
2	Input 2	22
3	Input 3	23
4	Input 4	24
5	Input 5	25
6	Input 6	26
7	Input 7	27
8	Input 8	28
9	Input 9	29
10	Input 10	30
11	Input 11	31
12	Input 12	32
13	Input 13	33
14	Input 14	34
15	Input 15	35
16	Input 16	36
17	Unused	37
18	Unused	38
19	Unused	39
20	Unused	40

JP13
40 Pin Dual Row Header
Digital Input - Bank 2 (17-32)
Pins 21-36 Common Buss

1	Input 17	21
2	Input 18	22
3	Input 19	23
4	Input 20	24
5	Input 21	25
6	Input 22	26
7	Input 23	27
8	Input 24	28
9	Input 25	29
10	Input 26	30
11	Input 27	31
12	Input 28	32
13	Input 29	33
14	Input 30	34
15	Input 31	35
16	Input 32	36
17	Unused	37
18	Unused	38
19	Unused	39
20	Unused	40

JP6
5mm Screw Terminals
Power and Serial

1	24v DC
2	GROUND
3	SHIELD
4	RxD
5	TxD

SECTION 7.0 CONFIGURATION JUMPERS

JP7 and JP8	1-2 = RS485 2-3 = RS232*
JP9	CLOSED = RS485 TERMINATION
JP10 and JP11	CLOSED = RS485 MASTER PULLUP/PULLDOWN

NOTES